AMD

AMD-768™

Peripheral Bus Controller

Revision Guide

Publication # **24472** Rev: **C**
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Revision History

Date	Rev	Description
March 2002	C	Added B2 silicon information.
February 2002	B	Initial public release.

AMD-768™ Peripheral Bus Controller Revision Guide

The purpose of the *AMD-768™ Peripheral Bus Controller Revision Guide* is to communicate updated product information on the AMD-768™ peripheral bus controller to designers of computer systems and software developers. This guide consists of four major sections:

- **Product Marking Identification:** This section, which starts on page 5, provides product types, product revisions, OPNs (Ordering Part Numbers), and product marking information.
- **Product Errata:** This section, which starts on page 6, provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification. A product errata may cause the behavior of the AMD-768 peripheral bus controller to deviate from the published specifications.
- **Revision Determination:** This section starts on page 15.
- **Technical and Documentation Support:** This section, which starts on page 16, provides a listing of available technical support resources. It also lists corrections, modifications, and clarifications to listed documents.

Revision Guide Policy

Occasionally, AMD identifies deviations from or changes to the specification of the AMD-768 peripheral bus controller. These changes are documented in the *AMD-768™ Peripheral Bus Controller Revision Guide* as errata. Descriptions are written to assist system and software designers in using the AMD-768 peripheral bus controller and corrections to AMD's documentation on the AMD-768 peripheral bus controller are included. This revision guide documents currently characterized product errata.

1 Product Marking Identification

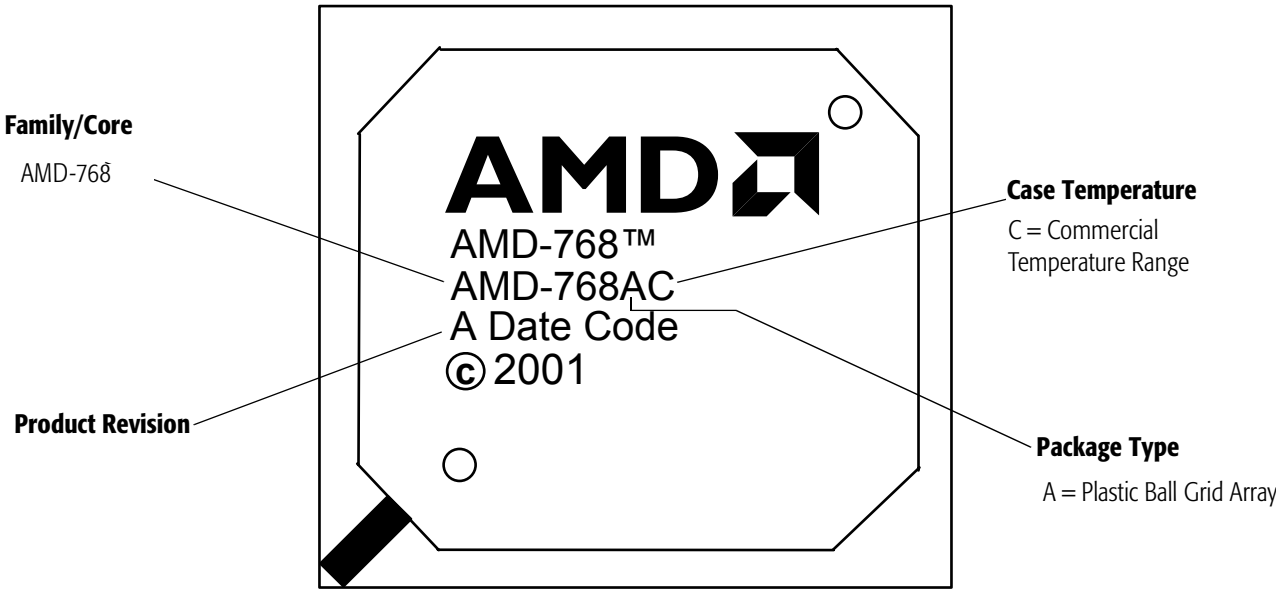

Table 1. Valid Ordering Part Number Combinations

OPN	Package Type	Operating Voltage	Case Temperature (max.)
AMD-768AC	492-pin PBGA	Logic core: 2.375-2.625V I/O core: 3.135-3.465V	85°C

Note:
Valid combinations are configurations that are or will be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

2 Product Errata

This section documents AMD-768 peripheral bus controller product errata. The errata are divided into categories to assist referencing particular errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 2 cross-references the revisions of the AMD-768 peripheral bus controller to each erratum. An "X" indicates that the erratum applies to the stepping. The absence of an "X" indicates that the erratum does not apply to the stepping.

Note: *There can be missing errata numbers. Errata that have been resolved from early revisions of the controller have been deleted, and errata that have been reconsidered may have been deleted or renumbered.*

Table 2. Cross-Reference of Product Revision to Errata

Erratum Number and Description	Revision Number	
	B1	B2
10 Multiprocessor System May Hang While in FULL APIC Mode and IOAPIC Interrupt is Masked	X	X
21 PCI Discard Card Timer Expiration Causes Data Corruption on PCI Primary Bus	X	X
22 Writes to Real Time Clock Must be Byte Width	X	X
23 AC '97 Modem Controller May Transmit Incorrect Data to AC-link	X	X
24 Single Processor Systems Will Not Resume from C2, C3, or POS Low Power States	X	X
25 PCI Bridge Does Not Handle Device Initiated Target Abort Cycles Correctly	X	X
26 USB Controller May Cause Secondary PCI Bus Contention	X	

10 Multiprocessor System May Hang While in FULL APIC Mode and IOAPIC Interrupt is Masked

Products Affected. B1, B2

Normal Specified Operation. The AMD-768 peripheral bus controller is designed to support FULL APIC mode in multiprocessor systems for system management events. If an interrupt is masked in the APIC controller of the AMD-768, then the corresponding interrupt message should not be sent to the processor via the 3-wire APIC bus.

Non-conformance. The AMD-768 peripheral bus controller will send an interrupt message via the 3-wire APIC bus regardless if the interrupt is masked or not.

Potential Effect on System. Since the processor had previously masked the APIC interrupt, it is not expecting to receive future APIC messages for the masked interrupt. The APIC controller will continuously send the interrupt message via the 3-wire bus until a processor accepts the message, causing the system to hang.

A system hang has been observed when executing a server shutdown command in Novell Netware versions 5.0 or 5.1 while using a serial mouse. During the server shutdown sequence, software writes an invalid CPU ID to the IOAPIC redirection table, and the system does not complete the shutdown.

Note: No failure has been observed when using a PS/2 mouse.

Suggested Workaround. None.

Resolution Status: No fix planned.

21 PCI Discard Card Timer Expiration Causes Data Corruption on PCI Primary Bus

Products Affected: B1, B2

Normal Specified Operation: The AMD-768 PCI bridge controller supports discarding PCI bus master cycles initiated on the primary PCI bus.

Non-Conformance: If a Primary PCI bus master does not retry a prefetchable cycle before the AMD-768 PCI bridge, the retry timer expires. The AMD-768 PCI bridge controller will supply corrupt data.

The Primary PCI bus master and the PCI bridge controller devices interact using the following sequence when transferring data.

1. A Primary PCI bus master initiates a memory read cycle to memory space on the PCI secondary bus.
2. The PCI bridge controller responds with a PCI retry cycle and continues to obtain the read data.
3. The Primary PCI bus master initiates a second memory read cycle at a different address than the first request.
4. The PCI bridge controller responds with a PCI retry cycle, since it is has the data for the first memory read cycle.
5. The Primary PCI bus master continues to retry the second memory read cycle.
6. Once the PCI bridge retry timer expires, the PCI bridge accepts the second memory read cycle from the Primary PCI bus master, but the PCI bridge did not completely flush its internal prefetch buffer from the first memory read cycle. The data supplied is corrupt.
7. The Primary PCI bus master retries the first memory read cycle and the PCI bridge completes the cycle, but the data supplied is corrupt.
8. All subsequent Primary PCI bus master reads are now completed with corrupt data. The system may hang.

Potential Effect on System: No impact on system functionality will occur when using the AMD-762™ system controller Northbridge. The AMD-762 Northbridge will not issue prefetchable reads downstream, nor will it retry a memory cycle to the AMD-768 Southbridge after the PCI retry timer has expired. Add-in cards on the Primary PCI bus perform prefetchable memory accesses only upstream to memory controlled through the Northbridge, not downstream through the Southbridge to memory residing on the secondary PCI bus.

Suggested Workaround: None.

Resolution Status: No fix planned.

22 Writes to Real Time Clock Must be Byte Width

Products Affected: B1, B2

Normal Specified Operation: The AMD-768 Real Time Clock function is designed to support byte- and word-width write operation to control registers and CMOS memory locations.

Non-Conformance: The AMD-768 Real Time Clock function does not support word width write operations to control registers and CMOS memory locations. If a word width operation is performed to PORT 70, then only the least significant byte is written.

Potential Effect on System: None.

Suggested Workaround: Use two byte-aligned cycles to perform write operations to RTC control registers and CMOS memory locations. The required sequence is:

Step 1: Software writes to PORT 70 the address index value as a single byte.
Step 2: Software writes to PORT 71 the data value as a single byte.

Similarly, use two byte-aligned cycles when PORT 72 is used for address index value and PORT 73 is used for data value.

Resolution Status: No fix planned.

23 AC '97 Modem Controller May Transmit Incorrect Data to AC-link

Products Affected: B1, B2

Normal Specified Operation: The AMD-768 AC '97 Modem Controller is designed to transfer either an even number or odd number of digital tone samples to the AC-link.

Non-Conformance: If the AC '97 Modem Controller transfers an odd number of samples and a register reset command is issued to the Modem Controller, the output data transmitted to the AC-link by the AC '97 controller may become corrupt.

Potential Effect on System: Data transferred from the PCI bus to the AC-link may become corrupt. The modem riser card CODEC transmits the corrupted data across the telephone line.

Suggested Workaround: None. The AC '97 modem is not supported in the AMD-768 peripheral bus controller.

Note: *This errata has no impact on the AC '97 audio function.*

Resolution Status: No fix planned.

24 Single Processor Systems Will Not Resume from C2, C3, or POS Low Power States

Products Affected: B1, B2

Normal Specified Operation: The AMD-768 Power Management controller is designed to support timer and PS/2 mouse and keyboard wakeups from the snoop cache capable clock control (C2) state, the non-snoop cache capable (C3) state, and the Power On Suspend (ACPI POS) states.

Non-Conformance: BIOS places the AMD-768 into virtual wire mode since it does not know if a single or multi-processor system is to be run. In this mode, the IO APIC and the legacy Priority Interrupt Controller (PIC) are enabled. Both interrupt controllers support interrupts as wake events.

In a single processor operating system, the IO APIC interrupts are masked when the system is placed into a low power state. The masking of the IO APIC interrupts inhibits a legacy IRQ from creating a resume event in power management state machine. The following legacy interrupts will not resume the system.

IRQ0 - Programmable Interval Timer (C2 and C3 state resume)

IRQ1 - PS/2 keyboard interrupt (POS state resume)

IRQ12 - PS/2 mouse interrupt. (POS state resume)

The Global status register located at offset PM28[IRQRSM_STS] bit is not set after a legacy IRQ event occurs which causes the power management logic to not resume the system.

Potential Effect on System: System will not resume from C2/C3 low power state. System will not resume from POS low power state by PS/2 keyboard or mouse.

Suggested Workaround: A software and hardware workaround exists for resuming from POS state but no work around is possible for C2/C3 state.

For POS state

Software work around: Before the ACPI complaint operating system places the system into a POS state, BIOS can disable the Advanced Priority Interrupt Controller (APIC) in the following sequence:

- BIOS clears [APICEN] bit (device B function 0 offset 4B'h) just before placing the AMD-768 into POS state
- The PS/2 keyboard and mouse IRQs will now resume the system from POS state
- Once the system has resumed BIOS can re-enable the APIC by setting [APICEN] bit

Hardware work around: Motherboard connects Super I/O PME output pin to AMD-768 ACAV input pin. BIOS enables ACAV_EN bit (General Purpose 0 ACPI Interrupt Enable Register) at offset PM22. BIOS enables PME output pin in Super I/O.

For software support, reference AMD application note: *Power Management Resume Support for the AMD-768™ Peripheral Bus Controller,* order #25818.

USB mouse and keyboard will awake system from Power On Suspend State.

For C2/C3 state

This workaround will not work for awaking from the C2/C3 state, since the operating system has full control. The (ACPI C2/C3) state support is not required for Microsoft®-compatible workstation and server platforms.

It is recommended that BIOS should disable the C2 state by

clearing bit C2EN (device B function 3 offset 4F'h). It is recommended that BIOS should disable the C3 state by clearing bit C3EN (device B function 3 offset 4F'h).

Resolution Status: No fix planned.

25 PCI Bridge Does Not Handle Device Initiated Target Abort Cycles Correctly

Products Affected: B1, B2

Normal Specified Operation: The PCI-to-PCI Bridge Architecture Specification Revision 1.1 states:

> If a Target-Abort occurs on the Primary interface when the bridge is acting as a bus master while forwarding a non-posted write transaction upstream, the bridge must:
> - Complete the corresponding data phase on the secondary interface by signaling a Target-Abort
> - Set the Received Target-Abort bit in the Primary Status register
>
> If a Target-Abort occurs on the Secondary interface when the bridge is acting as a bus master while forwarding a non-posted write transaction downstream, the bridge must:
> - Complete the corresponding data phase on the primary interface by signaling a Target-Abort
> - Set the Received Target-Abort bit in the Secondary Status register

Non-Conformance: If a Target-Abort occurs on the Primary interface when the bridge is acting as a bus master while forwarding a non-posted write transaction upstream, the AMD-768 PCI-to-PCI bridge:

- Transfers the first double word of the request followed by three extra data phases containing double words of FFFF_FFFF'h to the Secondary interface
- Does not signal a Target-Abort cycle on the Secondary interface
- Does not set (device A function 0 offset 04) bit RTA received target abort

If a Target-Abort occurs on the Secondary interface when the bridge is acting as a bus master while forwarding a non-posted write transaction downstream, the AMD-768 PCI-to-PCI bridge:

- Does signal a Target-Abort cycle on the Primary Interface, but no data is transferred to the Primary interface
- Does not set (device A function 0 offset 1C) bit RTA received target abort

Potential Effect on System: The system may hang if PCI adapter cards perform PCI target abort cycles whose destination is through the AMD-768 PCI-to-PCI bridge device.

Suggested Workaround: If a PCI adapter card executes a target abort cycle, then a catastrophic error has occurred. Either the PCI adapter card has a logical defect or software is attempting to access a location that the PCI adapter card has no knowledge of. The PCI adapter card should be removed from the system.

Resolution Status: No fix planned.

26 USB Controller May Cause Secondary PCI Bus Contention

Products Affected: B1

Normal Specified Operation: The AMD-768 Secondary PCI bus arbiter is designed to arbitrate PCI bus ownership between bus masters on PCI adapter cards and the internal USB host controller.

Non-Conformance: Secondary PCI bus contention will occur if a PCI adapter card and the internal USB controller interact in the following manner:

- The AMD-768 internal USB controller is enabled
- A PCI adapter bus master card relinquishes the PCI bus by deasserting its REQ# on the last clock of a transfer. The states of the following PCI signals are
  - FRAME# is de-asserted
  - Either STOP# or TRDY# are asserted
  - IRDY# is asserted
  - GNT# is asserted
- On the next PCI clock cycle the PCI adapter card initiates another bus mastering cycle by asserting FRAME#
- On the same cycle as FRAME# is asserted, the AMD-768 deasserts GNT#
- USB activity is pending within the AMD-768

Under these conditions the internal USB controller drives a PCI transaction onto the secondary PCI bus, resulting in PCI bus contention.

Potential Effect on System: Data corruption leading to eventual system hangs and failures. Long term component reliability problems due to bus contention.

Suggested Workaround: Disable the internal USB controller. BIOS can disable the internal USB controller by clearing bit 0 located at device B function 0 offset 48 (secondary PCI bus device enable register). Typical BIOS implementations provide a user setup option in the BIOS setup screen.

An external PCI-USB adaptor can be used if required.

Resolution Status: Fix planned for future silicon revision.

3 Revision Determination

The BIOS checks the PCI revision ID register for function 0h at offset 8h to determine the version of silicon as shown in Table 3.

Table 3. AMD-768™ Peripheral Bus Controller Revision IDs

Sequence	Revision	Device A Function 0h Offset 8h
4	B1	04h
5	B2	05h

4 Technical and Documentation Support

4.1 Documentation Support

The following documents provide additional information regarding the operation of the AMD-768 peripheral bus controller:

- *AMD-762™ System Controller Data Sheet*, order# 24088.
- *AMD-768™ Peripheral Bus Controller Data Sheet*, order# 24467.
- *AMD Athlon™ System Bus Specification*, order# 21902
- *AMD Athlon™ Processor BIOS, Software, and Debug Tools Developers Guide*, order# 21656
- *AMD Athlon™ MP Processor Model 6 Data Sheet*, order# 24685
- *Power Management Resume Support for AMD-768™ Peripheral Bus Controller Application Note*, order# 25818

For the latest updates, refer to www.amd.com and download the appropriate files. For documents under NDA, please contact your local sales representative for updates.